Remarks

Acceptance/formal entry therefor of this preliminarily submitted amendment prior to the Examiner taking up the above-identified application for a formal review is respectfully requested.

The originally submitted Specification was revised to correct discovered informalities therein. Several other revisions were implemented that are strictly of a minor grammatical nature. Due to the number of revisions being effected, applicants are submitting herewith a Substitute Specification (**Attachment A**) directed thereto. It is submitted, new matter is not being added therein, either by addition and/or deletion. As is required, a marked-up copy of the original Specification showing the changes being implemented therein is enclosed as **Attachment B**. Acceptance therefor of the Substitute Specification as a formal replacement of the originally submitted Specification is respectfully requested.

The status of the claims is presented hereinabove. Namely, there are currently pending claims 1-19, of which claim 1 is currently amended and claims 6-19 are newly presented. The revisions made to independent claim 1 are, basically, of a minor formal nature. In claim 1, line 2, the revision therein is strictly of a minor formatting nature and with regard to the two other revisions implemented in that claim, they are strictly grammatical corrections. The new claims are being presented, also, to more fully cover various originally disclosed inventive aspects directed to a semiconductor integrated circuit device which includes one or more field effect transistors such as a MISFET (or MOSFET) whose source and drain are characterized by an offset structure as well as others whose source and drain are characterized by a non-offset structure. This is further described below.

It is submitted, newly presented independent claims 6 and 15 are directed to a semiconductor integrated circuit device which is also inclusive of the types of MISFETs set forth in claim 1, but, however, are not necessarily limited to a SRAM scheme. In other words, it can be said that at least independent claims 6 and 15 of the newly presented claims are generic to a semiconductor integrated circuit device scheme as that set forth in claims 1+. Regarding a construction using both a MISFET in which the source and drain regions thereof are characterized by an offset structure as well as a MISFET in which the source and drain regions thereof are characterized by a non-offset structure, such as called for in claims 6 and 15, an example thereof is given with regard to Fig. 16, although not limited thereto. In Fig. 16 P-channel MISFET QL2 is characterized by an offset structure for the source and drain regions thereof and N-channel type MISFET Qt2 is characterized by a non-offset structure for the source and drain regions thereof, the non-offset structure also being of the LDD (lightly doped drain) type, consistent with claims 6+ and 15+. Another example of implementation of both a MISFET with an offset structure as well as another MISFET with a non-offset structure, the latter also being of the LDD type, is shown by Figs. 27(a) and 27(b). With regard to Figs. 27(a) and 27(b), it is noted that both the non-offset MISFET (Qp) as well as the offset MISFET (QL1, QL2) have a same channel conductivity type.

As can be seen from the dependent claims, a circuit construction such as that covered by independent claims 6 and 15 may also be of the type in which the MISFET(s) with an offset structure may correspond to an element in a SRAM cell of a memory array while the MISFET with a non-offset structure may constitute an element in a peripheral circuit (e.g., see Fig. 9(b)). An example construction of a SRAM cell of a semiconductor integrated circuit device is detailed with regard to Fig. 11 and Figs. 14-24, in which the MISFETs with the thickened lines in Fig. 11, for example, represent MISFETs in which the

source and drain regions thereof have an offset structure. Detailed discussion regarding a MISFET with an offset construction as well as a MISFET with a non-offset construction is given extensively in the Specification in conjunction with the example embodiments described and illustrated.

Examination as well as favorable action on the currently pending claims 1-19 as well as an early formal notification of allowability of the above-identified application is respectfully requested.

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Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

Larry N. Anagnos
Reg. No. 32,392

LNA/dks
(703) 312-6600
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